IN THE SPECIFICATION:

Please replace paragraph [0036] with the following amended paragraph:

--The data driving circuit according to the present invention includes a timing controller 3, a level shifter ~~(not shown in FIG. 4)~~ 4, a plurality of digital to analog converters ~~5a and 5b~~ 5a, 5b, and 5c, a plurality of amplifiers ~~7a, 7b to 7n and 8a, 8b to 8n~~ 7a, 7b to 7n, 8a, 8b to 8n, and 10, 10b to 10n, a plurality of 2x1 multiplexers 9a, 9b to 9n, a common voltage amplifier (not shown), and a power supply (not shown).--

Please replace paragraph [0037] with the following amended paragraph:

-- The timing controller 3 formats input data such as display data R, G and B having, for example, one bit, four bits, or six bits, vertically and horizontally synchronized signals Vsync and Hsync, a clock signal DCLK and a control signal DTEN, and outputs the formatted data to the gate and data drivers so that the gate and data drivers display a picture image. Also, the timing controller 3 outputs a selection signal to select an appropriate converter to be driven. The level shifter 4 amplifies the voltage levels of the clock signal DCLK and the control signal DTEN among the signals output from the timing controller 3. Then, a plurality of digital to analog converters ~~5a and 5b~~ 5a, 5b, and 5c convert the signals output from the timing controller 3 to analog signals according to each gray level, for example, 64 gray (6 bit) and 2 gray (1 bit). The plurality of amplifiers ~~7a, 7b to 7n and 8a, 8b to 8n~~ 7a, 7b to 7n, 8a, 8b to 8n, and 10, 10b to 10n amplify the signals output from the respective digital to analog converters ~~5a and 5b~~ 5a, 5b, and 5c. Then, the plurality of 2x1 multiplexers 9a, 9b to 9n selects one of the amplified signals

output from the ~~first and second~~ first, second, and third digital to analog converters ~~5a and 5b~~ 5a, 5b, and 5c based on the selection signal of the timing controller 3, and then outputs the selected signal to the LCD panel. The common voltage amplifier amplifies a common voltage, and supplies the common voltage amplified to the LCD panel.--

Please replace paragraph [0038] with the following amended paragraph:

-- The timing controller 3 includes a frame memory. The first digital to analog converter 5a obtains a multigray (64 gray (6 bit)) image, ~~and~~ the second digital to analog converter 5b obtains a low gray (2 gray (1 bit)) image. If there is a third digital to analog converter ~~(not shown)~~ 5c in addition to the first and second digital to analog converters 5a and 5b, then the first digital to analog converter 5a obtains a multigray (64 gray (6 bit)) image, the second digital to analog converter 5b obtains intermediate gray (16 gray (4 bit)) image, and the third digital to analog converter 5c obtains a low gray (2 gray (1 bit)) image.--

Please replace paragraph [0039] with the following amended paragraph:

--~~Also, if there are three digital to analog converters,~~ Thus, a plurality of 3x1 multiplexers is formed, each of which selects one of three input signals, and then outputs the selected signal.--